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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,348	11/30/2001	Richard K. Spielberger	H0002128-US	5523

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,348	SPIELBERGER ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) 20-23 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 and 24-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 November 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election / Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-19 and 24-27, drawn to a ball grid array mounted circuit classified in class 174, subclass 260.

   II. Claims 20-23, drawn to a method for electrically interconnecting an electronic component to a printed circuit board, classified in class 29, subclass 832.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process such as the heating step is not required in the product. Further, the steps of providing fixture and loading the solder ball into the fixture are not required in the product.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group II is not required for Group I, restriction for examination

purposes as indicated is proper. During a telephone conversation with Dennis Bremer (Reg. 40,528) on December 10, 2002 a provisional election was made with traverse to prosecute the invention of a ball grid array mounted circuit, claims 1-19 and 24-27. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-23 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

5. The drawings are objected to because the figures are improperly cross hatched. All of the parts shown in section, and only those parts, must be cross hatched. The crosss hatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the parts. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear what is meant by "flexible polyimide like material". The examiner considered flexible material.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al., US Patent 5,973,930, hereafter Ikeda.

Regarding claim 1, Ikeda discloses a ball grid array mounted circuit comprising:

a stress relief substrate having a top surface and a bottom surface; spaced conductive vias extending between the top surface and said bottom surface; connection pads at said top surface with each connection pad capturing at least one of said vias; connection pads at said bottom surface in registration with said connection pads at said top surface (package bearing substrate 6 with pad 14 and 15. Though the vias are not explicitly disclosed but they are inherently there for electrical connection from one side to the other, see figure 1, column 3, line 25 to column 4, line 7);

an electronic component having a first thermal coefficient of expansion and having connection pads spaced to align with said connection pads at said top surface; first solder connection formed from solder balls between said connection pads at said top surface and said component connection pads (semiconductor package 10 with pads 13 and solder ball 5, see figure 1);

a printed circuit board having a second TCE and having connection pads aligned with said connection pads at said bottom surface; second solder connections formed from solder balls between said connection pads at said bottom surface and said PCB connection pads, wherein said first solder connections and said second solder connections are shaped to absorb at least a portion of stress due to differences between said first TCE and said second TCE (wiring board 9 with pads 16 and solder ball 8, see figure 1).

Regarding claim 8, Ikeda further discloses the package having TCE of about 7 ppm/degree C and PCB in the range of about 20-30 ppm/degree C, column 3, line 45-67.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al., US Patent 5,973,930, hereafter Ikeda, as applied to claim 1 above, and further in view of Jackson et al., US Patent 6,333,563, hereafter Jackson.

Regarding claim 2, though Ikeda does not explicitly disclose about the flexibility of the material used for the stress relief substrate, use of such flexible material is known in the art to reduce the thermal strain induced stress on the solder balls. Jackson discloses one such organic interposer in the range of between about 1.5 to about 3mm; see Jackson, column 3, line 5-20. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the assembly of Ikeda with a flexible polyimide as taught by Jackson in order to reduce the thermal strain induced stress on the solder balls.

Regarding claim 11, the combination of Ikeda and Jackson further discloses the said conductive vias are located in said flexible substrate only at said connection pads, see Ikeda figure 1.

12. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al., US Patent 5,973,930, hereafter Ikeda, as applied to claim 1 above, and further in view of Osaka et al., US Patent 4,897,918.

Regarding claim 3 and 4, the applicant is claiming the relative size of the pads on component and printed circuit board and that on the stress relief substrate. Though, Ikeda does not disclose such relationship between the pads, it is known in the art for better controlling the stress in the system. Osaka disclose such comparatively smaller pads on the middle substrate than that on the component and board to have better stress control, see Osaka figure 14. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the assembly of Ikeda with the pads on component and printed circuit board larger than that on the stress relief substrate for better stress control.

13. Claims 5, 6-7, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al., US Patent 5,973,930, hereafter Ikeda as applied to claim 1 above.

Regarding claim 5, though Ikeda does not disclose the connection pad at said top surface capture plurality of said conductive via, such multiple via connected to a single pad is known in the art for better solder ball strength. Further, such multiple via connection on a pads are used for better heat dissipation rate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the assembly of Ikeda with the connection pad at said top surface capture plurality of said conductive via in order to have better solder connection.

Regarding claims 6 and 7, the applicant is claiming the via diameter and the pitch of the same. However, the diameter of the via will depend upon the method of producing the same and also the method of filling the via, such as very small via can be made by laser. Further, it will be difficult to fill small via holes and a balance is to be maintained to have economical method of achieving the goal. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the assembly of Ikeda with the via having the diameter and pitch as claimed in claims 6 and 7 in order to have the required via connection with reasonable cost.

Regarding claims 9 and 10, the applicant is claiming the type of semiconductor package used, chip scale package, as claimed in claim 9 and a ruggedized die as claimed in claim 10. However, the crux of the invention of Ikeda is to control the stress / strain during the thermal cycle of the device to avoid damage to the system and though Ikeda disclose a semiconductor device in general, the teaching can be used for any

semiconductor device and package. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the teaching to provide the assembly of Ikeda with chip scale package, as claimed in claim 9 and a ruggedized die in order to have controlled stress / strain during thermal cycle.

14. Claims 12-19 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ikeda et al., US Patent 5,973,930, Jackson et al., US Patent 6,333,563, hereafter Jackson and Osaka et al., US Patent 4,897,918, as applied to claims 1-11.

Regarding claims 12 and 24, the combination of Ikeda, Jackson and Osaka disclose all the feature of the claimed invention including the larger pad connection at the component pads and PCB pads as applied to claims 1, 3 and 4 above.

Regarding claims 13 and 25, the combination of Ikeda, Jackson and Osaka disclose all the feature of the claimed invention including the material and thickness of the substrate as applied to claim 2 above.

Regarding claim 14, the combination of Ikeda, Jackson and Osaka disclose all the feature of the claimed invention including the conductive pads at said top surface capture a plurality of said conductive pad as applied to claim 5 above.

Regarding claims 15,16, 26 and 27, the combination of Ikeda, Jackson and Osaka disclose all the feature of the claimed invention including the via diameter and pitch and pad size as applied to claims 6 and 7 above.

Regarding claim 17, the combination of Ikeda, Jackson and Osaka disclose all the feature of the claimed invention including the TCE of the package and PCB as 7 ppm/degree C and 20-30 ppm/degree C as applied to claim 8 above.

Regarding claim 18, though the combination of Ikeda, Jackson and Osaka does not disclose the via uniformly spaced throughout said flexible substrate, it is economical to have such universal substrate which can be used with various system with different solder pad spacing and can be kept ready to use with various devices. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the modified assembly of Ikeda with the substrate with the via uniformly spaced throughout said flexible substrate in order to reduce the cost of the assembly.

Regarding claim 19, the combination of Ikeda, Jackson and Osaka disclose all the feature of the claimed invention including the vias in the flexible substrate located at said connection pads at the top surface as applied to claim 11 above.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Alagartnam et al., flexible interposer with the hole diameter from 20 to 400micron with a pitch of 1mm.

Behfar disclose a connector with plurality of conductive column captured by a single solder ball.

Lin discloses an assembly with hour glass shaped solder connection for increased fatigue life.

Kimbara et al., disclose a plastic package with a pad capturing plurality of via for better solder connection.

Arai, Lee et al., Kresge et al., and Vafi et al., discloses various stress relief interposer for semiconductor assembly.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
December 14, 2002

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